SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

L3035 - L3036-L3037 MONOCHIP SLICs

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CONTENTS

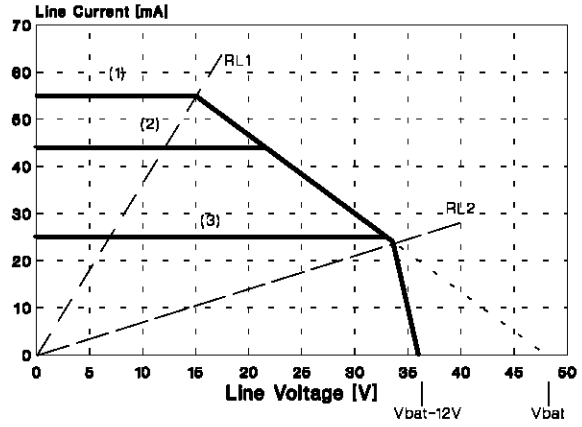
1. DC PERFORMANCES

1.1 DC FEEDING CHARACTERISTICS

1.1.1 Active Mode: (D0 = High, D1 = High)

Three different feeding regions are present (see Fig.1) and the operation point is related to the Line Resistance (length) to be fed.

Figure 1: Line Current vs. Line Voltage



1) Current Limiting Region.

Line Resistance > 0
Line Resistance < RL1 (Maximum Res. for Limiting region)

A constant current is supplied to the Line,indipendently of the Line Resistance .
The value of the current is selected out of three values according to the status of the control input ILIM:

ILIM	FEED CURRENT
Low	25mA
NC	44mA
High	55mA

2) Resistive Feeding Region.

Line Resistance > RL1
Line Resistance < RL2 (Maximum Res. for Resistive region).

The DC feeding behaves as a Voltage Generator with an RFEED Equivalent Series Resistance:the current is not constant as in the Limiting region, but decreases proportionally to the Line resistance.

This dependency allows the AGC operation on telephone side.

Equivalent Voltage Generator:

V = VBAT

RFEED = RDC/10 + 2RP

RDC/10 : synthesized DC resistance

2RP : series of two protection resistors

3) Low Impedance Region.

Line Resistance > RL2

The synthesized DC resistance becomes very low and the DC feeding,seen at TIP and RING Pins,behaves as an ideal voltage generator.
Seen at TIP and RING Terminals,a series resistance is added, due to protection resistors,connected between pin and terminal.

Equivalent Voltage Generator:

V = VBAT-12V

RFEED = 2RP

This region has been provided,not just for the low out impedance itself,but in order to have a 12V drop when Line Current is 0mA: it is necessary condition to allow sufficient output swing in ON-HOOK Transmition.

Varying with continuity the Line Resistance,from the Short to the Open Circuit,the three regions are passed through,without discontinuities of operation,changing from one to another.
AC operation is not affected and the correct functionality is not corrupted at the corners.

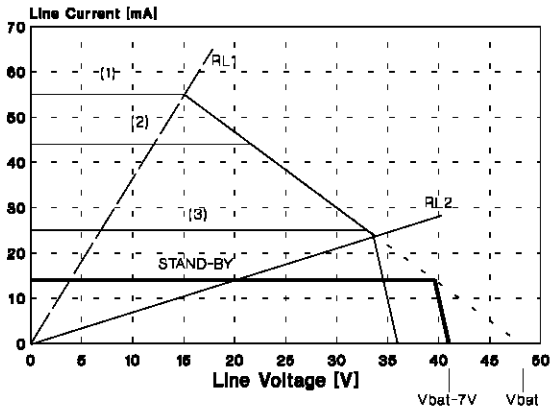
1.1.2 DC Feeding in Stand-by Mode.

(D0=High, D1=High)

In Stand-By mode,a constant current of 14mA is fed to the line (see Fig.2) up to the end of limiting region.
Then, a 0Ω impedance is shown at Tip and Ring output pins: the output impedance seen at Line-Card terminals is due to protection resistors Rp in series to the line.

A Vdrop 7V is still present when Il=0mA.

Figure 2: Line Current vs. Line Voltage



1.2 FORMULAS AND CALCULATION

- Feed Current: IFEED = f (RL)

Limiting	ILIM
Resistive	VBAT/(RFEED+RL)
Low Imp.	(VBAT-12V)/(2RP+RL)

- Feed Resistance :

The value is defined by an external resistor RDC according to the formula:

RFEED = RDC/10 + 2RP

RDC =10 · (RFEED - 2RP)

- Maximum Line Resistance in Limiting region.

IL = VBAT/(RFEED+RL)
ILIM = VBAT/(RFEED+RL1)

RL1 = VBAT/ILIM - RFEED

Known the R/Km of the wire,the formula give the max length of the line that can be feeded with constant current.

- Maximum Line Resistance in Resistive region.

At the corner Resistive-Low Imp. must be:

IL = VBAT / (RFEED + RL)

and

IL = (VBAT-12) / (2RP + RL) -->

VBAT / (RFEED+RL2) = (VBAT-12) / (2RP+RL2)

developing:

RL2 = [VBAT · (RFEED-2RP)/12] - RFEED

Depending on values of ILIM, RFEED and RP the DC charcteristic of L303X shows different shapes: it can start with Limiting region and continue through Resistive and Low Impedance or start directly with Resistive or start in Limiting and entering directly to Low Impedance, without passing through the Resistive region.

Following examples will clarify the subject:

Example 1.

VBAT=48V RFEED=900Ω RP=50Ω

If ILIM= 56mA

RL1 = VBAT/ILIM - RFEED.

RL1 = 48/(56E-3) -900 < 0Ω (DC char. starts in Resistive region)

RL2 = [VBAT*(RFEED-2RP)/12] - RFEED.

= [48 · (900-100)]/12 -900=2300Ω

IL2= VBAT/(RFEED+RL2)

= 48/(900+2300)=15mA

If ILIM=43mA

RL1= 48/(43E-3) 900=216Ω

RL2=2300Ω

If ILIM=25mA

RL1= 48/(25E-3) -900=1020Ω

RL2=2000Ω

Example 2.

VBAT=48V RFEED=400Ω RP=60Ω

If ILIM=56mA

RL1=48/(56E-3) -400=457Ω

RL2=[48 · (400-120)]/12 -400=720Ω

IL2=48/(400+720)=42.85mA

When ILIM=43mA or ILIM=25mA , as their value is <IL2=42.85mA or very closed to this value,the DC charactristics will directly change from Limitation to Low Impedance region.

In this case:

RL2=(VB-12)/ILIM -2RP

If ILIM=43mA

RL2=(48-12)/(43E-3) -120=720Ω

If ILIM=25mA

RL2=(48-12)/(25E-3) -120=1320Ω

Given the Length of a Line and the Resistance per Km ,with the a.m. formulas the calculation of the operating point is immediate and also the definition of the DC feeding parameters.

1.3. SIGNALING

- OFF/HOOK detection.

When Stand-By or Active mode is set, the L303X monitors the status of the Line,forcing the output ODET (pin 18) of the Logic Interface as follow:

ODET = HIGH ON/HOOK

LOW OFF/HOOK

On the Line Card,when the controller detects ON-OFF/HOOK conditions it performs different operations, according to the status of the Slic:

SLIC STATUS	OPERATION
Stand-by	Forces L303X in Active mode when OFF/HO OK is detected
Active before conversation	Monitors ODET for dialing
Active during conversation	Stops conversation when ON/HOOK condition is detected, forcing the two Slics in Stand-By.

The OFF/HOOK condition is detected by sensing the Transversal DC current flowing from TIP to RING ,Line drive outputs.

When this current is higher than a threshold of 10mA, ODET is forced Low; 0.5mA below that threshold ODET returns High.

No low-pass filtering is provided: ODET output has to follow in real time the status of the Line .

Common Mode Current is not affecting the status of ODET.

Note: in RINGING mode,ODET signals the RING-TRIP detection; the subject will be further described in §.6.

- GND KEY detection.

When a DC common mode current ILL [defined as ILL= (IB-IA)/2 with IA=current sourced from TIP and IB=current sunk into RING] is greater than 5mA, the Ground Key condition is detected and the output OGK (pin20) of Logic Interface is forced Low.

As the Line,normally, can be coupled to Common Mode AC sources (Mains),in order to give immunity to GND KEY detection, a Low-Pass filtering is provided to the sensing circuit.
For that purpose, the CRT capacitor connected between CRT (pin17) and AGND is used.

The same capacitor and circuitry is used for RING TRIP detection (see § 6).

Note:

- OGK is not affected by the Transversal component.
- When TIP and RING have a DC conduction to GND with a Transversal component (|IA| ≠ |IB|), the OFF/HOOK condition is also detected (ODET=Low).

1.4 TIP OPEN MODE.

In Tip Open mode , with GST (pin21) input High, TIP is set in High Impedance and RING only can drive the Line.

RING output current capability is limited to 30mA.

With Line open the output voltage is typically :

VRING= VBAT + 4.5V = - 43.5V

In L3037, GST also controls the Polarity Reversal: see control interface table in §4.

2. AC PERFORMANCES.

The complete AC model of L303X Slic appears in Fig.3. In this § ,as a tutorial chapter,we refer to the simplified model of Fig. 4, for the AC parameters calculation.

In such a model the capacitors CCOMP (loop stability) and CAC (separation of AC from DC component of Line current) are not considered. In speech band in fact CAC can be considered a

Figure 3.

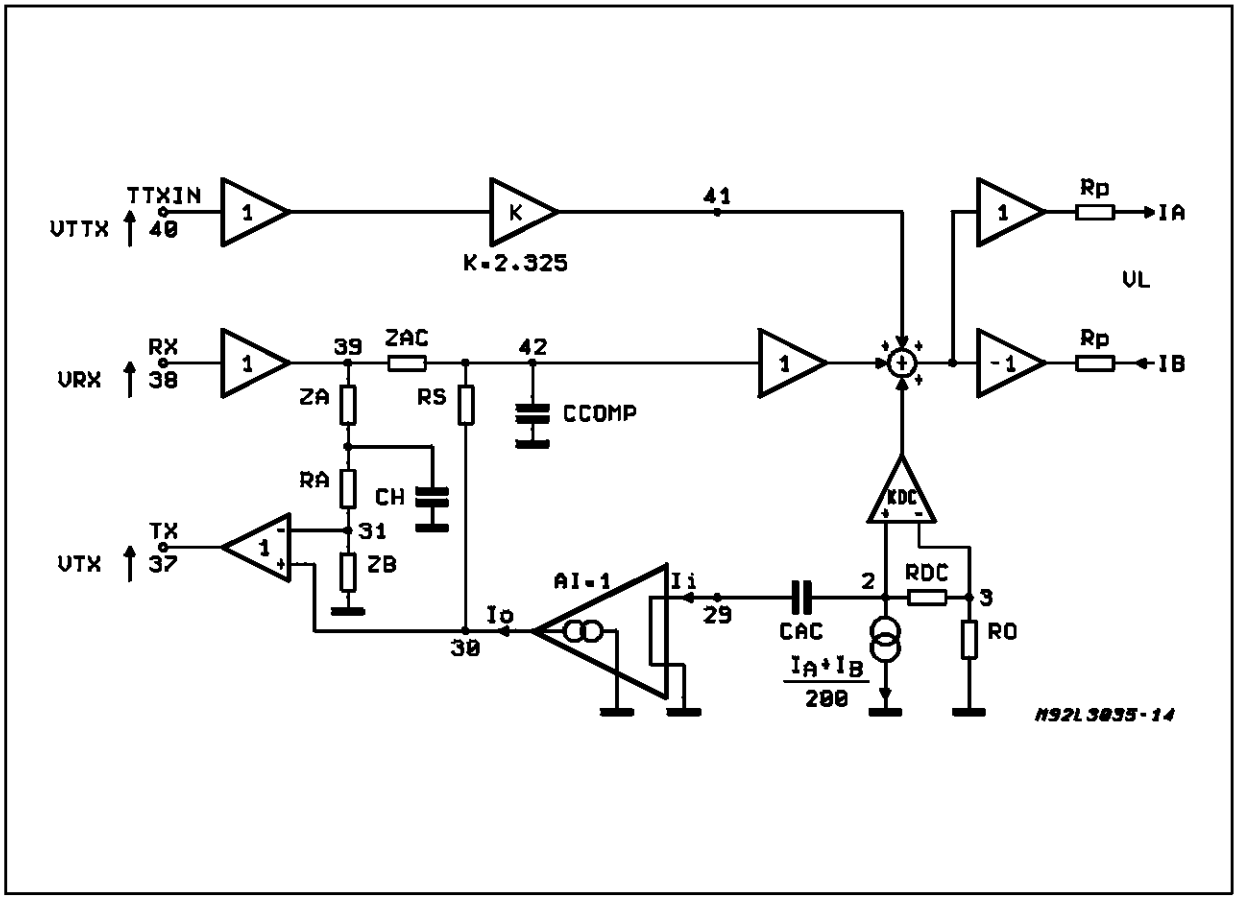
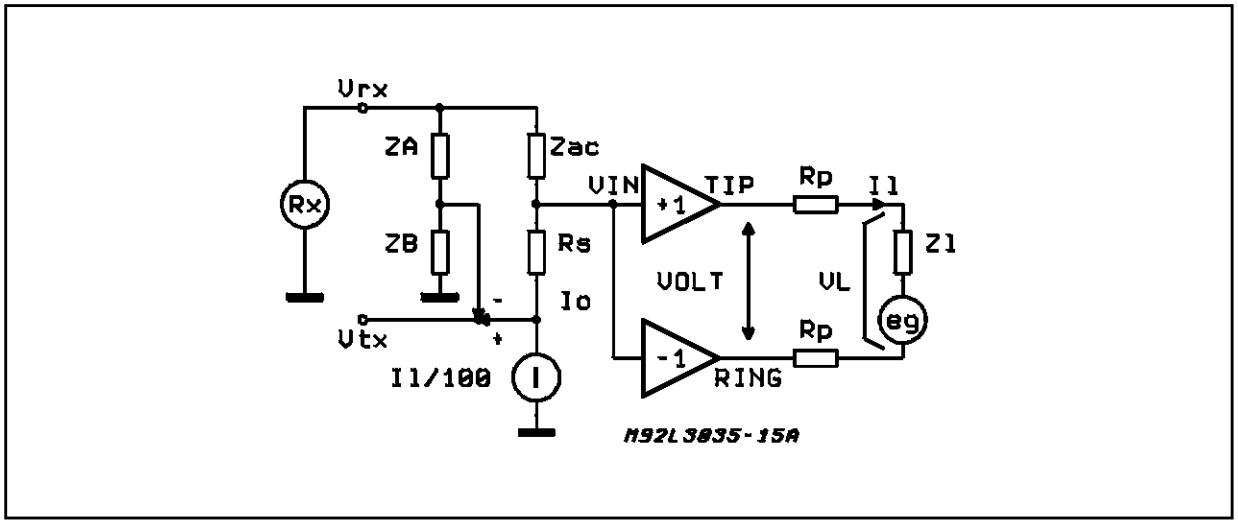


Figure 4.



short circuit and CCOMP an open circuit. The metering cancellation network RTTX and CTTX is also not considered.

SPICE simulation will show their influence on the AC performances (see AN501).

2.1 IMPEDANCE SYNTHESIS.

L303X provides an active synthesis of AC output impedance real or complex:

VOUT= 2 · VIN=2 · ZAC · IL/100

ZTR = VOUT/IL = ZAC/50 Equivalent Impedance at TIP-RING pins of the IC.

Considering the protection resistors Rp,the impedance shown to the Line is:

ZS= ZTR + 2Rp

2.1.1 Examples (ZRL = Return Loss Test Impedance)

a)ZRL =600Ω
Rp=40Ω
ZS= ZTR + 2Rp = ZRL
ZTR = 600Ω-80Ω
ZAC = 50 · ZTR =26KΩ

b)ZRL =220Ω + (820Ω//115nF) (GERMANY)
Rp=40Ω
ZS = ZTR + 2Rp = ZRL
ZTR = 220Ω + (820Ω//115nF) - 80Ω
ZAC = 50 · ZTR= 7K + (41K//2.3nF)

c)ZL =900Ω + 2.12µF (USA)
Rp=62Ω

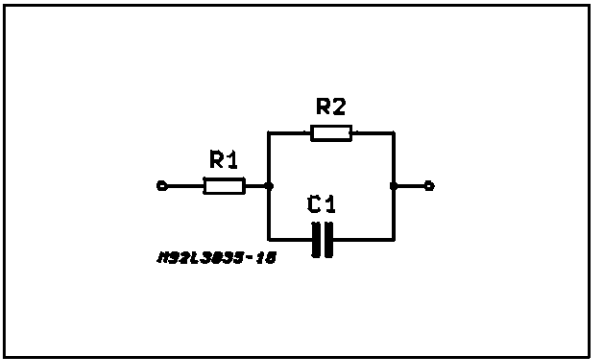
In principle, ZAC should be calculated as follow:
ZS = ZTR + 2Rp = ZRL
ZTR = 900Ω + 2.12µF - 124Ω
ZAC = 50 · ZTR=38.8K + 42.4nF

In fact this impedance cannot be used because, due to the internal chip architecture, the ZAC has to provide a DC path between pin 42 and pin 39 and it is not possible with a capacitor in series.

A different ZAC* has to be used and it must be equivalent inside the speech band (same amplitude and phase),in order to fulfill R.L. requirements.

The simplest network ZAC* that can replace the original one is shown in fig. 5.

Figure 5.



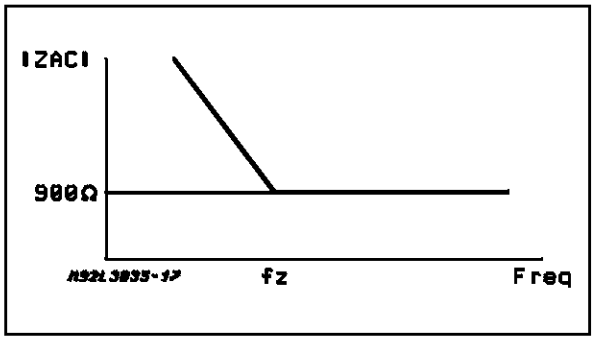
Calculation of ZAC*:

ZAC= R + C = 38.8K + 42.4nF

ZAC(ω)= (1+jωRC) / jωC ω = 2πf

The Bode diagram (see Fig. 6) shows a Zero at:
fz= 1/2πRC= 96.7 Hz

Figure 6.



ZAC* = R1 + (R2// C1)

ZAC*(ω)=(R1+jωC1R1R2+R2)/ (1+jωC1R2)
ω = 2πf

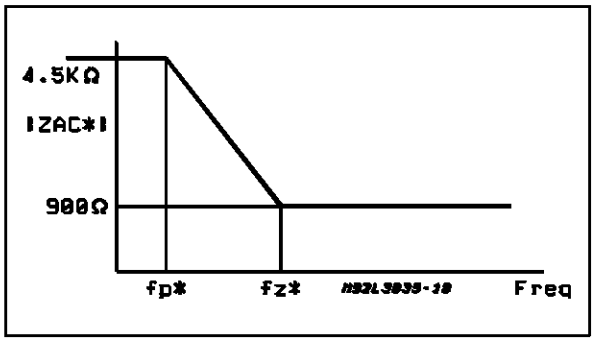
The Bode diagram shows pole at

fp*= 1/ (2πR2C1)

and zero at

fz* = (R1+R2)/ 2πC1R1R2

Figure 7.



From the conditions to be met :

R1= R

fz*= fz

R1+R2= RT

RT=225K

(RT is the resistance between pin 39 and pin 42; its value is related to the max allowed offset due to the input leakage current)

We obtain:

R1= R	R1= 38.8K
R2= RT-R	R2= 225K-38.8K= 186.2K
C1= C * RT/(RT-R)	C1= 51.2nF

Note that fp*= 1/2πR2C1= 16.7Hz affects ZAC* at very low frequency,outside the speech band. Inside the band, ZAC* can be considered with same frequency response as ZAC.

2.2 RECEIVE GAIN.

GRX= VL / VRX = 2 · [ZL / (ZL + ZS)]

GRX = 1 (0dB) if ZL = ZS

2.3 TRANSMIT GAIN.

GTX = VTX / VL (with VRX=0)

VTX = (IL / 100) · (ZAC+RS)
= [(VL / ZS) / 100)] · (ZAC+RS)

GTX = VTX / VL = (1/2) · [(ZAC + RS) / (ZS · 50)]
= (1 / 2) · [(ZAC + RS) · (ZAC + 50 · 2Rp)]

GTX = 1 / 2 (-6dB) if RS=50 · 2Rp

2.4 TRANSHYBRID LOSS.

THL = VTX / VRX (with EG = 0)

VTX = [VRX - (ZAC + RS) · IL / 100] - VRX · ZB / (ZA+ZB)

= [VRX - (ZAC + RS) · (VRX · GRX / ZL) / 100)] - VRX ZB / (ZA + ZB)

and :

THL = (ZL + 2 · RP - RS / 50) / (ZL + 2 · Rp + ZAC / 50) - ZB / (ZA + ZB)

TH L = ZL / (ZL + ZS) - ZB / (ZA+ZB)

THL = 0 if ZB / (ZA + ZB) = ZL / (ZL + ZS)

ZA = K · ZS
ZB = K · ZL

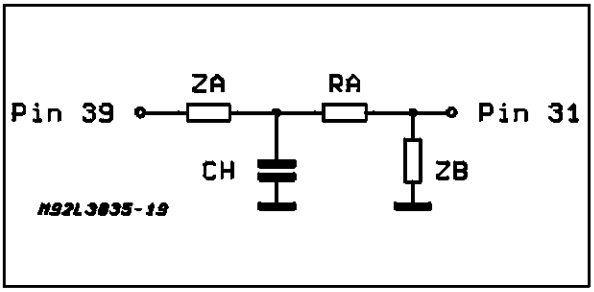
In fact it is reccomended to use K = 50, same scaling factor of ZAC

ZA = 50 · ZS = ZAC + RS

ZB = 50 · ZL

The capacitor Ccomp has not been considered. In fact, when high THL performances are required, Ccomp has to be taken in account. In that case the cancelling network of Fig 8A has to be used, where CH is the image of Ccomp.

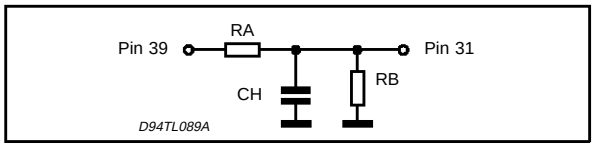
Figure 8A.



Where:
ZA = 50 · ZTR = ZAC
RA = 50 · 2Rp = RS
ZB = 50 · ZL
CH = Ccomp

NOTE: when ZL is the same specified in Gain and Return-Loss measurements, the cancelling network can be simplified as in Fig. 8B

Figure 8B.



Where:RA = RB = 50 · |ZL|
CH = Ccomp
The component count is reduced and THL performances are, in many case, acceptable.

Figure 9.

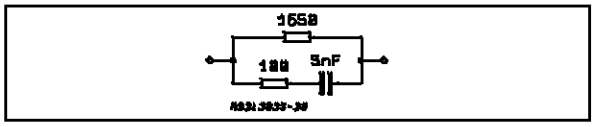
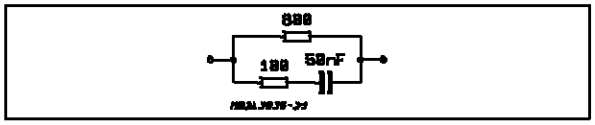


Figure 10.



2.4.1 Example

ZA and ZB calculation for USA:
ZL1 (fig. 9) and ZL2 (fig. 10) represent the two THL test networks.
$R_P = 62\Omega$

ZL1 = 1650Ω // (100Ω + 5nF) Loaded Line

ZL2 = 800Ω // (100Ω + 50nF) Unloaded Line

ZA = ZAC = 38.8K // (186.2K + 51.2nF)

RA = RS = 50 · 2Rp = 6.2K

ZB1 = 50 · ZL1= 82.5K // (5K + 100pF)

ZB2 = 50 · ZL2 = 40K // (5K + 1nF)

2.5 AC SIGNAL SWING AND DC CHARACTERISTIC ADJUSTMENT.

Quite often an optimization of the AC swing capability of L303X when operating with very long lines or low battery voltages is requested.

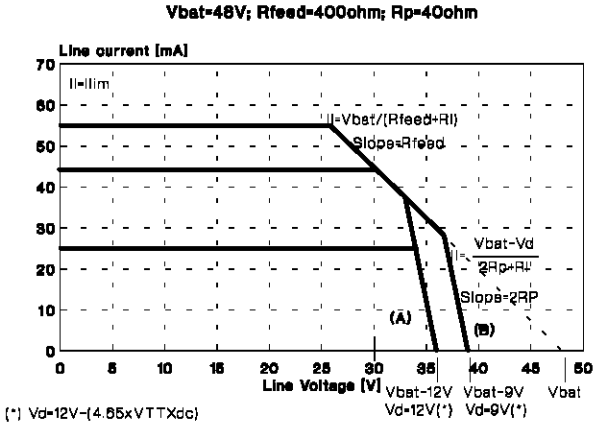
The following example will clarify about the subject. Let's calculate the output swing available in the condition:

IL = 21mA R-Loop = 600Ω Rp=50Ω VBAT=-24V

1) First of all the DC Feeding characteristic (see Fig. 11) must be modified.

To have the requested feeding current,the voltage drop must be reduced from 12V to 9V. The DC characteristic is translated from (A) to (B) by

Figure 11.



forcing at pin 40 a DC offset Voff:

Voff = (12V - 9V) / 4.65 = 645mV (see fig. 3)

With IL = 21mA the Slic operates in the DC Low Impedance region.

2) AC swing .

Figure 12.

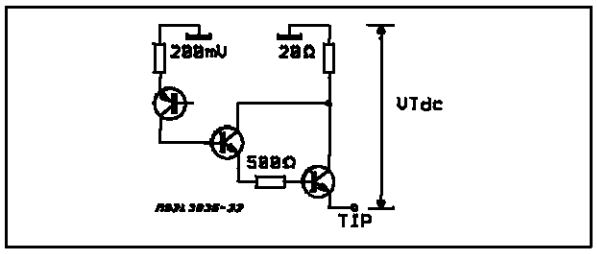


Fig. 12 shows a simplified schematic diagram of TIP output stage.

The DC voltage on TIP output is:

VTdc = -(9V - 1.7V) / 2= -3.65V

where 9V is the total voltage drop referred to the battery voltage (after a.m. modification of DC characteristic) and 1.7V is the VCE of external transistor in the resistive region.

Considering the circuit in Fig. 12 the maximum voltage that TIP can reach is:

VTmax = -(200mV + VSAT + VBE + 500Ω · IL/Hfe + VBE)

= -(200 + 100 + 700 + 100 + 700)mV

= -1.8V

Therefore the max AC peak we can get is:

VTpk = 3.65V - 1.8V = 1.85V

The same,in the opposite direction, is for RING output. So the peak voltage between TIP and RING available is:

VTRpk = 3.7V

This level is available at IC pins; at line terminals a lower value,due to protection resistors Rp,must be considered:

suppose ZL = 600Ω

VLpk = VTRpk · [ZL / (ZL+2Rp)] = 4.0V · [600 / (600+100)] = 3.2V

3. METERING PULSE INJECTION.

L303X provides an input (TTXIN pin 40) for Tele-Tax metering pulse injection. In §2.5 you can see how this pin can be used also for DC characteristic adjustment.

Typically the metering pulse is a 12KHz or 16KHz sinusoidal burst, with shaped start and stop, in order to minimize the interference in the phonic band.

In order to reduce the echo on TX stage and achieve a low output impedance, the cancellation network Zttx = Rttx + Cttx is provided in the 4 wire transmission path.

When Zttx matches the line impedance Z1 (at TTX frequency) the echo is minimized and the output impedance, is 2RP (due to protection resistors only).
Mismatching imply an increase of echo and output impedance

Fig. 13 and Fig. 14 show the equivalent model concerning the injection and cancellation of metering signal

Calculation of the cancellation network:

Vl = 2K · (1-G) · [(Zac + Rs) / Zac] · Vttx

where: G = [1 + Zac / K · Zttx] / {1 + Zac / [(Zl + + 2Rp) · 50]}

and K=2.3

the target is: Vtx = 0

that means: G = 1 ----> Zttx = 50 (Zl + 2Rp) / K

Note: higher attenuation of the TTX echo can be achieved; the simplest way is Low-Pass filtering the TX signal.

Figure 13.

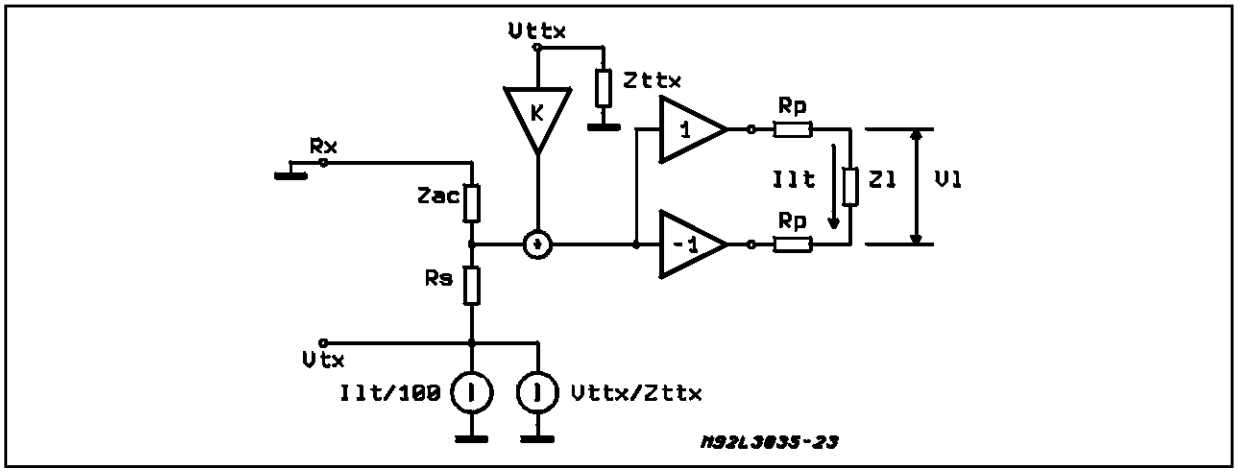
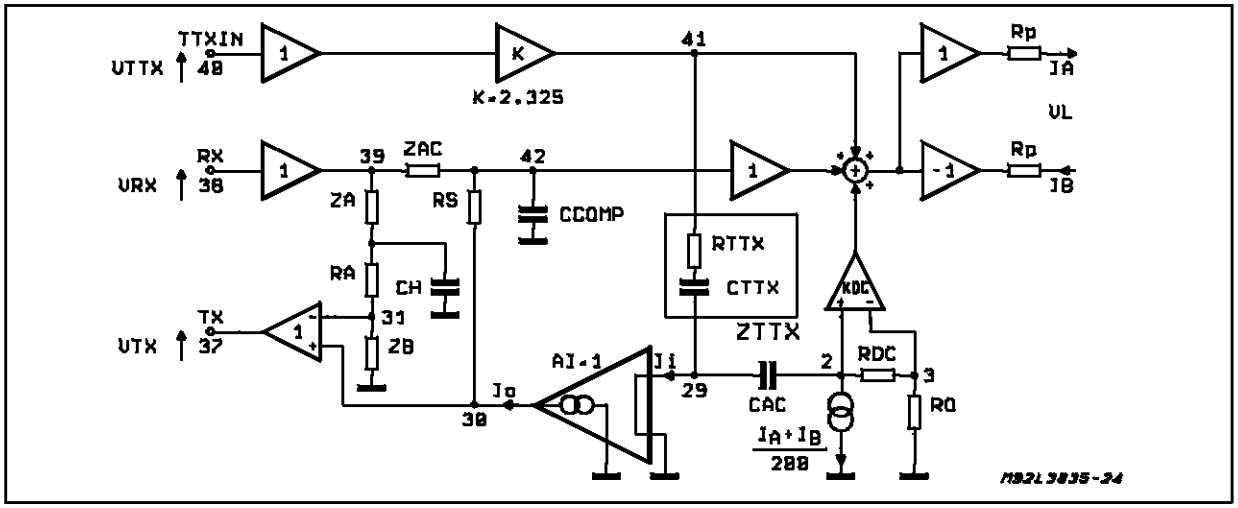


Figure 14.



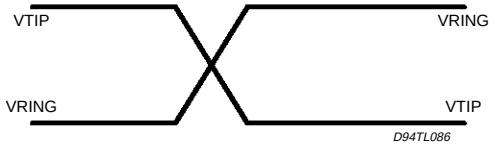
4. REVERSE POLARITY (L3037 only)

L3037 version provides the Reverse Polarity mode, selected by the control interface combination:

	D0	D1	GST	LIM
STAND-BY R.P.	1	1	1	X
ACTIVE R.P.	1	0	1	X

Reverse Polarity is not available in Ringing mode

AC characteristics are not affected; only the polarity of the DC voltage between Tip and Ring is reversed.
A linear shaped transition, see following figure, which dV/dT is defined by the capacitor CREV connected between the pin CREV and AGND, highly reduces the crosstalk level compared to a step reversal.



The CREV capacitance, depending on the dV/dT value, is given by the formula:

CREV = K / (dV / dT)
where $k = 2 \cdot 10^{-4}$ (± 10%)

NOTE: when the R.P. feature is not used, CREV pin must be grounded to AGND.

5. LONGITUDINAL BALANCE.

5.1 TRANSVERSAL TO LONGITUDINAL CONVERSION (T/L).

The transversal to longitudinal conversion ratio is defined in this way:

Tlc = 20·log (Vx / Vl) as shown in fig. 15

The ratio Vx / Vrx is indipendent from the AC feedback, in fact it depends from the line signal and it doesn't take in account the absolute value of line voltage. This ratio depends on the matching of the output amplifiers gain K1 and K2 and on the mismatch of the protection resistors.
The Tlck due to the mismatch of the of the output amplifiers gain can be computed as follows:

Vx = V · (K1 - K2) / 2

$$Vl = (K1 - K2) \cdot \frac{R}{R + Rp}$$

$$Tlck = 20 \cdot \log(Vx / Vl) = 20 \cdot \log\left(\frac{K1 + K2}{K1 - K2} \cdot \frac{Rp + R}{2R}\right) \quad (1)$$

The Tlce due to mismatch of the external protection resistors is :

$$Tlce = 20 \cdot \log \frac{E \cdot Rp}{2R} \quad (2)$$

Where E is the mismatch between Rp1 and Rp2
Rp1 = Rp(1 - E) and Rp2 = Rp(1 + E)
The complete formula of the transversal to longitudinal conversion is:

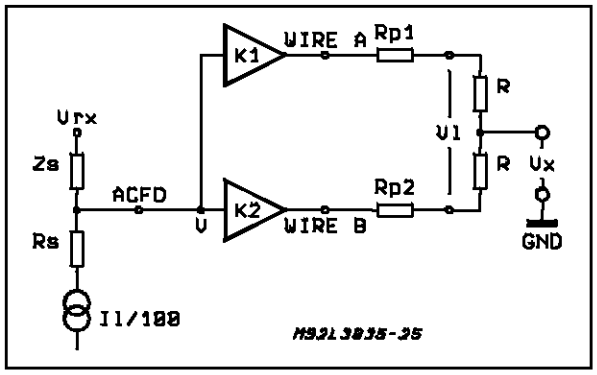
$$Tlc = 20 \cdot \log\left(\frac{K1 + K2}{K1 - K2} \cdot \frac{Rp + R}{2R} + \frac{E \cdot Rp}{2R}\right) \quad (3)$$

Note:
When the SLIC is in current limiting the unbalanced DC path provides an additional contribution. In that case the transversal to longitudinal conversion becomes:

$$Tlc = 20 \cdot \log\left|\frac{K1 + K2}{K1 - K2} \cdot \frac{Rp + R}{2R} + \frac{E \cdot Rp}{2R} + i\frac{Xc}{2R} \cdot \frac{Greg}{200}\right| \quad (4)$$

Where: Greg = 14
$Xc = 1/(2 \cdot \pi \cdot f \cdot Cac)$

Figure 15: Transversal to longitudinal conversion.



5.2 LONGITUDINAL TO TRANSVERSAL CONVERSION (L/T)

The longitudinal to transversal conversion ratio is defined as:
$Ltc = 20log\left(\frac{Vl}{Vin}\right)$ as shown in fig. 16.

where: $It = \frac{K \cdot (I1 + I2) + I1 - I2}{2}$; $Zac = Zs - 2Rp$

The transversal current value, It, depends on the precision reached by the current mirror circuit and on the mismatch of the two protection resistors.
The "Ltc"due to the mismatch of the internal circuit (K) is:

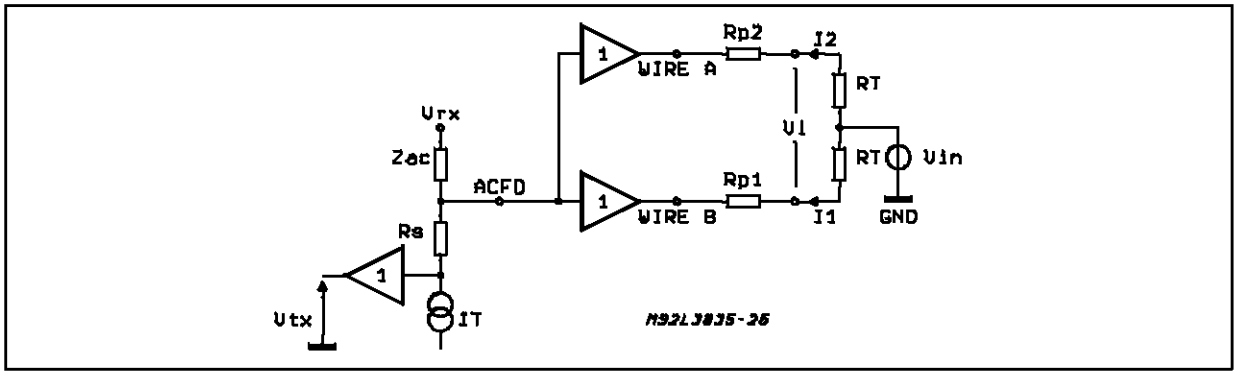
$$Ltck = 20log(K \cdot \frac{Zac}{Rt + Rp} \cdot \frac{Rt}{Rt + Rp + Zac/2})$$

The "Ltc"due to mismatch of the external protection resistors is:

$$Ltce = 20log(2E \cdot \frac{Rp}{Rt + Rp} \cdot \frac{Rt}{Rt + Rp + Zac/2})$$

Where E is the mismatch between Rp1 and Rp2
Rp1 = Rp · (1 + E) Rp2 = Rp · (1 - E)

Figure 16: Longitudinal to transversal conversion



Therefore the complete formula is:

$$Ltc = 20log\left(\frac{K \cdot Zac \cdot Rt + 2E \cdot Rp \cdot Rt}{(Rt + Rp) \cdot (Rt + Rp + Zac/2)}\right) \qquad (4)$$

K ≤ 1.75 E -3 for L3036
K ≤ 0.75 E -3 for L3035

Example:

L3036 Rp = 40Ω 1% tolerance (E = 0.01), Zac = 520Ω, Rt = 300Ω

Assuming worst case for L3036 K = 1.75 E- 3

from the (4)

$$Ltc = 20log\frac{273 + 240}{204E3} = -52dB$$

6. RINGING.

With L303X an external ringing generator that injects the signal in the line through a relay is needed.

The Slic provides:

- Drive relay capability
- Activation/Deactivation of relay, syncronous with zero-crossing of ringing signal.
- Ring-Trip detection

L303X enters Ringing-Mode with the control inputs:

D0 = LOW D1= HIGH

When the ringing relay is activated REL (pin26) is forced Low and TIP and RING output stage become voltage generators, with current limitation, able to source and sink the line current injected by the external ring generator.This current,internally processed,allow the Slic to detect the status of the line (ON-OFF/HOOK).

6.1 RINGING INJECTION.

Different ways to inject the ringing signal are possible:

a)Battery backed (see Fig. 17)
The ring generator has one terminal connected to the battery. TIP current only is sensed for Ring-Trip detection.

b)Earth referred (see Fig. 18)
Dual configuration of a). The ring generator has one terminal connected to GND. RING current only is sensed for Ring-Trip detection.

c)Balanced (see Fig. 19).
The ringing signals injected on TRIP and RING wires are in phase opposition. SLIC terminals are disconnected from the line: Ring-Trip detection is obtained from additional hardware.

§ 6.4 will describe the subject.

Figure 17.

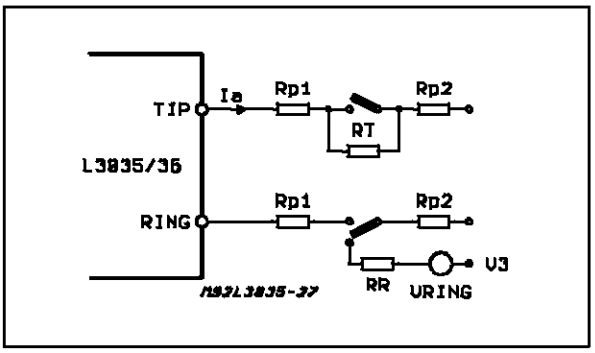


Figure 18.

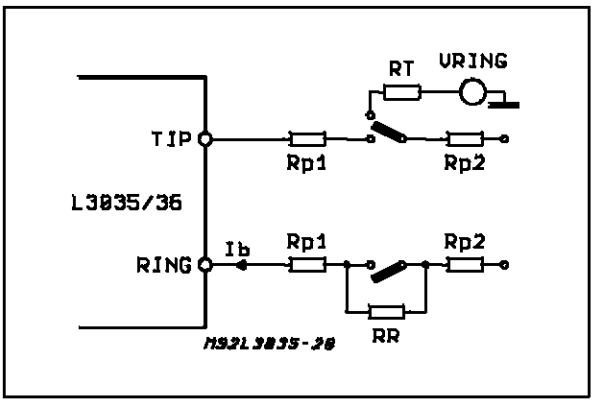
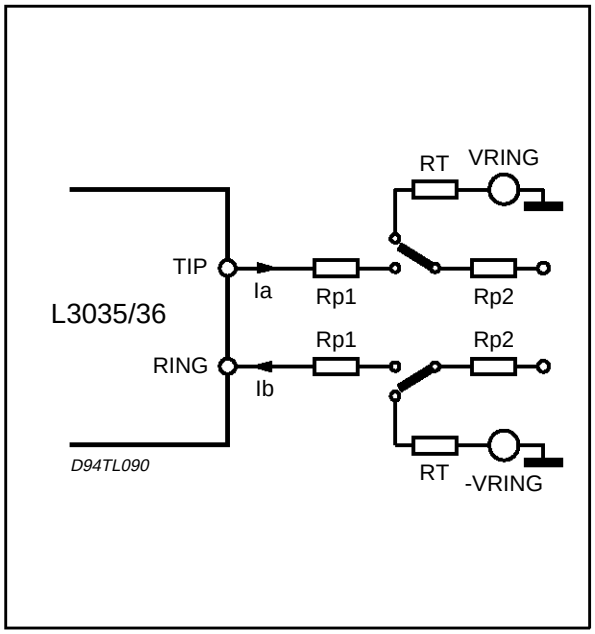


Figure 19



6.2 RING-TRIP DETECTION.

Ring-Trip condition is detected by sensing the currents Itip and Iring (see Fig. 20)

It = (Itip + Iring)/2

When the DC component of It >5mA the Ring-Trip condition is detected and L303X reacts:

- deactivating the ringing relay :REL (pin26) forced High
- forcing ODET (pin18) at Low level (OFF/HOOK).

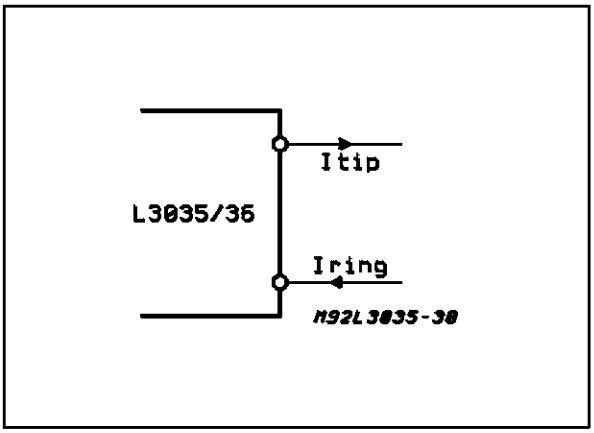
REL and ODET are latched and do not change opening the current loop. To leave this status Active Mode (D0=High D1= Low) has to be entered or in general, change status. Although the Ring-Trip detection uses ODET to signal the status of the line, there is a substantial difference respect to the ON-OFF/HOOK detection in Stand-By and Active mode.

In Ring-Mode and ON-HOOK condition an AC current is present in line: the Ring-Trip detection must ignore it and be dependent on the presence of a DC component only. The Ring-Trip detector reject the AC component by integrating the line current.

The detection threshold can be reached only if Il has a DC component. The consequence is that the response is not immediate (as in Stand-By or Active) but takes some delay time that is dipendent on the DC current value (i.e. line length).

AC rejection and delay time depends on capacitor CRT (Ring-Trip Capacitor) connected between pin17 and GND.

Figure 20.

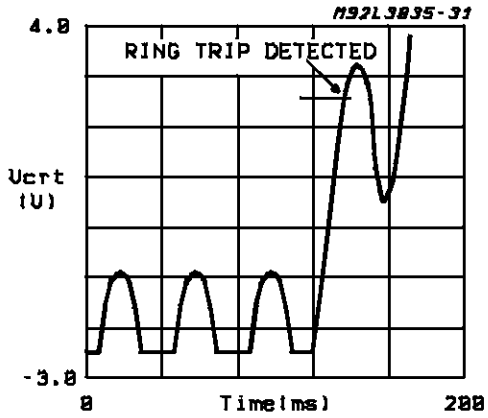


6.2.1 CRT calculation.

Referring to the battery backed case,the Ring-Trip is detected by integration the line current (sensed on Tip wire) on the CRT capacitor.

When the voltage on the capacitor exceedes 2.5V,the Ring-Trip is detected (see Fig. 21)

Figure 21.



CRT should be selected in order to avoid that during one half sinewave cycle, in On/Hook,its voltage Vcrt exceeds +2.5V (Ring-Trip Threshold).

Fig. 22 shows the correspondence between the CRT charging current Icrt and the line current I_L.

In Fig. 23 and Fig. 24 are reported the Line current and the CRT charging current Icrt, referred to the case:

Line Length = 1Km Load = 2 REN Freq.= 25 Hz
Vring = 60Vrms
suppose CRT charged during one half-cycle with Icrt =100µA, its value must be:

CRT(100µA · 20ms) / 5V = 400nF

Of course this is a worst case, supposing I_L > 20mA for the whole half-sinewave. An optimized value will be lower and be calculated considering

the I_L in the worst condition:
maximum REN#, shortest loop,maximum ring level.

Figure 22.

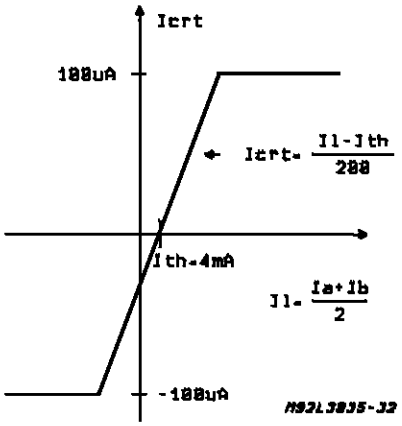


Figure 23.

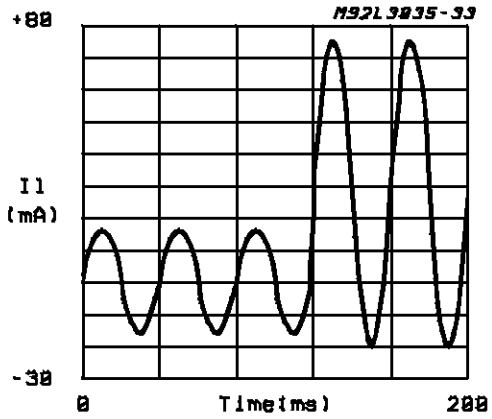
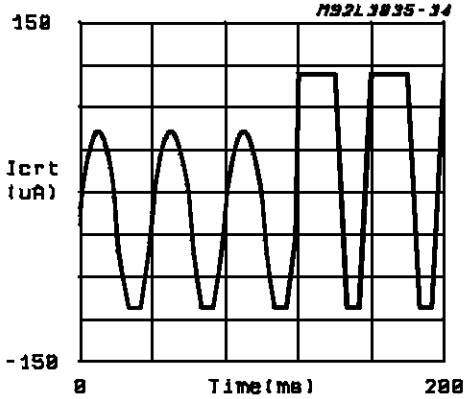


Figure 24.



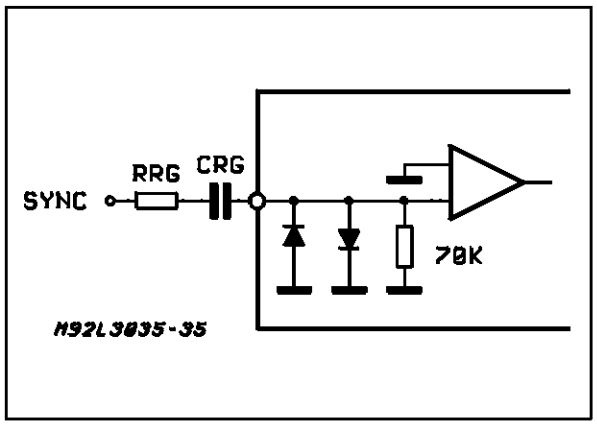
6.3 RELAY DRIVE SYNCHRONIZATION.

L303X provides the possibility to synchronize the activation and deactivation of the relay with the zero-crossing of the ringing signal.
The synchronization improves the reliability of relay and reduces the level of interferences induced in the adiacent lines.

The synchronization is locked to the zero-crossing of the voltage signal at RGIN input (pin15) (see Fig. 25).

The current flowing in RGIN input has a positive phase respect to SYNC sinusoidal voltage,due to the RC impedance (RRG and CRG) in series.
The zero-cross at RGIN anticipates the SYNC zero-cross with the possibility to compensate the activation time of the relay.
Depending on the signal used as SYNC, three possibilities of synchronization can be considered: (we refer to the battery backed solution but the concept is general)

Figure 25.



1) Line Voltage Synchronization (see Fig. 26):
SYNC = Ringing Generator Voltage

Activation and deactivation of relay happen at ZERO VOLTAGE condition.

RRG = (Vring / 25µA) · cos(2 Fring · T 180°)

CRG = 25µA / [Vring · sin(2 Fring · T 180°) · 2πFring]

T = Relay response time
Fring= Ringing Frequency

2) Line Current Synchronization (see Fig. 27):

SYNC = Voltage drop on Tip side (image of the Line Current)

Activation of relay is not synchronized : before activation the synchronizing signal is disconnected. Activation happen immediately after L303X enter in Ringing Mode (D0 = Low D1 = High).

Deactivation happens at ZERO CURRENT condition.

RRGC = RRG / K

CRGC = CRG · K

where: K= |ZR| / RT

Figure 26.

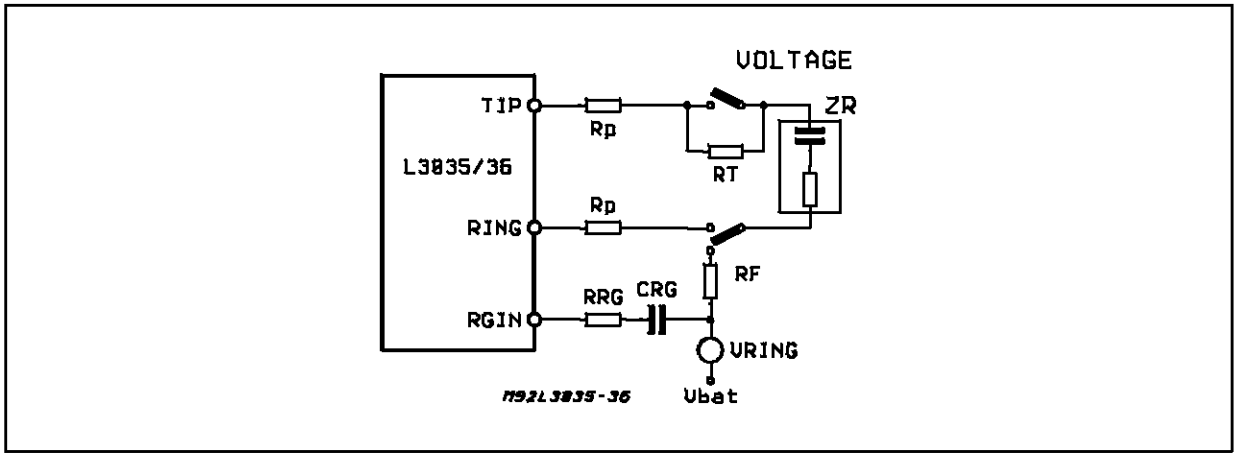


Figure 27.

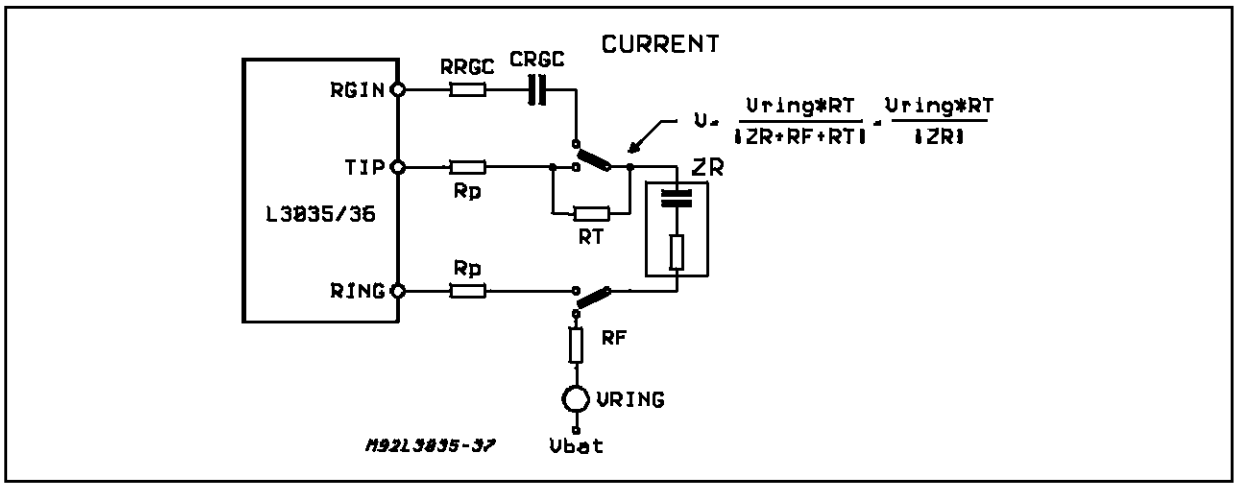
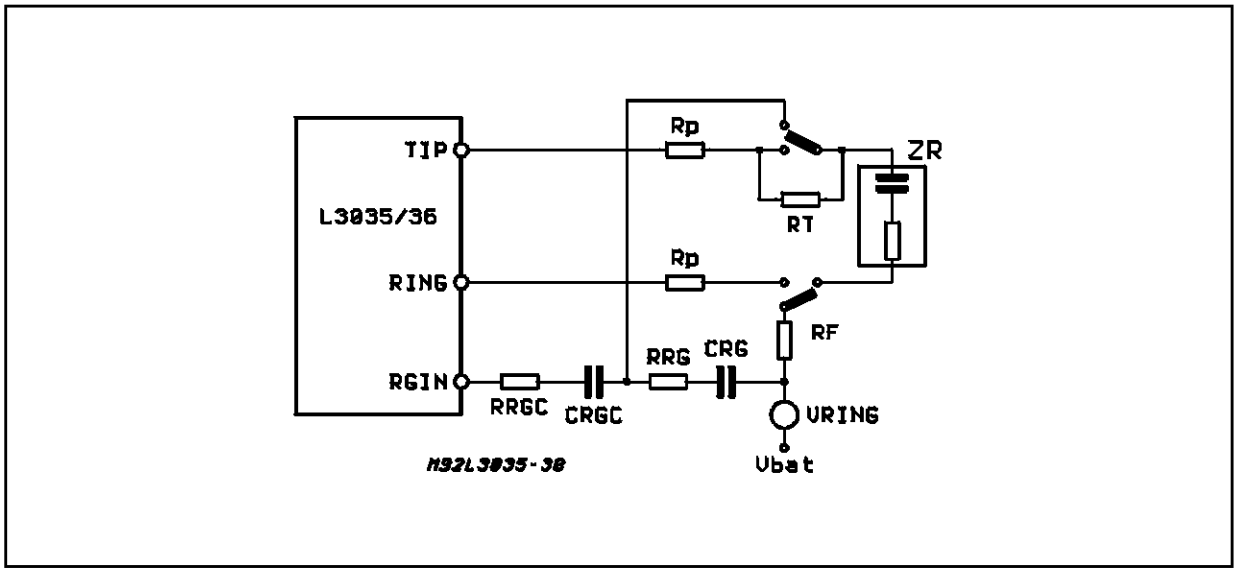


Figure 28.



3) Voltage and Current Syncronization (see Fig.28):

Activation takes place at ZERO VOLTAGE condition and deactivation happens at ZERO CURRENT condition.

RRGC = RRG / K

CRGC = CRG · K

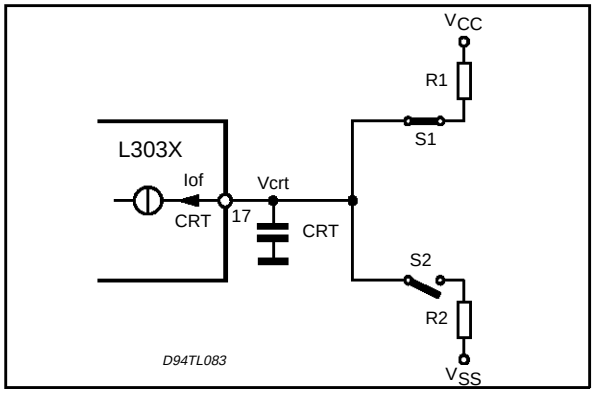
where: K = |ZR| / RT

6.4 BALANCED RINGING: Ring-Trip detection.

6.4.1 General information.

Although specifically designed for unbalanced Ringing injection, L303X can be adapted, with additional hardware, in order to manage the Ring-Trip detection with balanced injection.

Figure 29: Shows the Basic Equivalent Circuit



When the Line current is positive the switch S1 is On and S2 Off and the capacitor CRT is charged through the pull-up resistor R1. When the Line current is negative S1 is Off and S2 On,and CRT is discharged through the pull-down resistor R2.

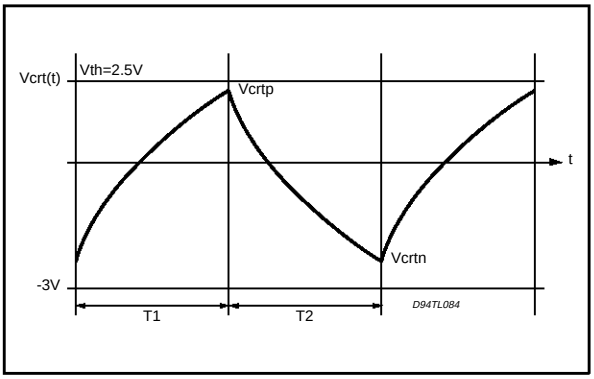
The internal current generator,at pin 17 (CRT) of L303X,sinks a current Iof of about 15µA to produce a negative voltage offset on CRT capacitor. When IL=0, both S1 and S2 are off,and the current generator forces CRT at a negative level that is clamped at -3V.

The voltage Vcrt(t) is a periodic waveform (see Fig.30) with exponentially shaped edges,that swings between a maximum (Vcrtp) and a minimum (Vcrtn) peaks that depend on Vcc, Vss, R1, R2, T1, T2 and Iof.

In On-Hook,T1=T2=T,and Vcrt must stay below a threshold Vth=2.5V to prevent Ring-Trip detection.

In Off-Hook,T1 > T2, Vcrt drifts up and Vcrtp must exceed Vth = 2.5V in order that L303X will detect a Ring-Trip.

Figure 30.



6.4.2.Calculation.

An approach is now given in order to properly calculate the value of R1,R2 and CRT that are functions of:

Battery Voltage	VBAT
Positive Voltage	Vcc
Negative Voltage	Vss
Ringing Level	Vrng
Ringing Frequency	Frng

To make the calculation easy let's refer to the particular case:

Vcc = -Vss = V and R1= R2 = R

Basically CRT and R are calculated through a successive approximation procedure that develops in three steps .

Step 1: suppose Iof=0 ,define a time constant R · CRT in order to have Vcrt with a peak value VM= V/2 (one half of the voltage swing available)
It corresponds to a condition half way between a very short and a very long time-constant

In case of very short time-constant Vcrt would be a square wave,reaching the maximum level available, producing a ring-trip detection anyway,regardless to the Hook status:it's a condition to be absolutely avoided.

In case of very long time-constant,Vcrt will be a continous level (due to the heavy low-pass filtering on ringing frequency) depending on the hook status. Ring-Trip detection should be possible but the detection time will be too long.

If T1 is the time duration of positive half wave and T2 of the negative,and given:

K1= -T1 / RC and K2= -T2 / RC

the positive and negative peaks of Vcrt, VM and Vm are given by:

a) $VM = V \cdot [1-2e^{K1} + e^{(K1+K2)}] / [1-e^{(K1+K2)}]$

b) $Vm = -V \cdot [1-2e^{K2} + e^{(K1+K2)}] / [1-e^{(K1+K2)}]$

In On-Hook: T1 = T2 = T and K1 = K 2 = K

and the formulas are simplified:

c) $VM = V \cdot [1-e^{K}] / [1+e^{K}]$

d) $Vm = -V \cdot [1-e^{K}] / [1+e^{K}] = -VM$

From c) comes the value of K:

$K = Ln[(V-VM) / (V+VM)]$

Given the ringing frequency and fixed a CRT value comes the first approximation value of R:

$R = - T/(K \cdot CRT)$

Step 2 : Iof is now taken in account.
The influence of Iof is to add a negative DC offset on Vcrt waveform (in step 1 has been considered the AC component) wich value is:

$VDC = -R \cdot Iof$

The real peak voltage of Vcrt is:
$Vcrtp = VM - R \cdot Iof$
In On-Hook, to avoid ring-trip detection we have to meet the condition (with 0.5V of margin):

$Vcrtp < Vth - 0.5V = 2.0V$

If the condition is not satisfied CRT value and R value must be modified:
to reduce Vcrtp must be reduced CRT and increased R (the contrary to increase it).

Besides, the internal Ring-Trip circuit of L303X needs, to detect a Ring-Trip, that a negative level of -3.0V has been previously present on CRT pin.
The condition is met if:
$Vcrtn = Vm - R \cdot Iof = -VM - R \cdot Iof < -3V$
If the condition is not met, Vcrtn can be reduced increasing R and reducing CRT.

Step 3 : Ring-Trip detection:
in Off-Hook the presence of a DC component in the line current increases the time duration T1 and decreases T2 according to the formulas:

$T1 = T \cdot [1+(2/\pi) \mid \sin^{-1} (Vbat / \sqrt{2}\, Vrng) \mid]$
$T2 = T \cdot [1-(2/\pi) \mid \sin^{-1} (Vbat / \sqrt{2}\, Vrng) \mid] = 2T-T1$

were: Vbat = battery voltage
Vrng = rms value of ringing voltage
T = 1/(2 · Frng) half period of the ringing signal

The value of VM calculated from formula a) gives the peak value of Vcrt in Off-Hook,that has to meet the condition:

$Vcrtp = VM - R \cdot Iof > Vth+0.5V = 3.0V$

in order to guarantee a ring trip detection (with a margin of 0.5V).
If the condition is not met,the wanted limit can be reached with a grater VM value :in that case a lower time constant must be adopted.

Example.

Given: Fmg = 50Hz |VBAT| = 48V Vmg = 60Vrms
Vcc = -Vss = V = 5V

1): $K = Ln[(V-VM) / (V+VM)] =$
$= Ln[(5-2.5) / (5+2.5) = -1.1$

choosen a CRT=220nF

$R = -T / (CRT \cdot K) = 10ms / 220nF \cdot 1.1 =$
$41.4K\Omega$
(R = 43K2 will be next considered).

2): The negative offset is:
$Vdc = -R \cdot Iof = -43K\Omega \cdot 15\mu A = -645mV$
and the positive and negative peak value in On-Hook:

$Vcrtp = VM + Vdc = 2.5 - 0.645 = 1.85V$
$Vcrtn = Vm + Vdc = -2.5 - 0.645 = -3.15V$

The values meet the conditions:

$Vcrtp < 2.0V$ and $Vcrtn < -3.15V$.

3): Off-Hook condition:

$T1 = T \cdot [1 + (2/\pi)\sin^{-1} (Vbat / Vrng) =$
$= 10ms (1 + 0.64 \sin^{-1} (48 / 85) =$
$= 10ms \cdot 1.38 = 13.8ms$

$T2 = 2T - T1 = 20 - 13.8 = 6.2ms$
$K1 = T1 / R \cdot CRT = 13.8 / 9.46 = -1.46$
$K2 = T2 / R \cdot CRT = 6.2 / 9.46 = -0.66$

from a): $VM = 5 \cdot [1-2e^{(-1.46)}+e^{(-1.46-0.66)} /$

$/ (1-e^{(-1.46-0.66)} = 3.69V$
$Vcrtp = VM - Vdc = 3.69 - 0.645 = 3.05V$

Also this parameter fulfils the requirement for ring trip detection:
$Vcrtp > 3.0V$

Note: in case of iteration,to easily reach the solution,two concepts have to be kept in mind:

- fixed a time constant,the negative DC offset increases with the R value.
- fixed an R value,reducing the time constant increases the peak to peak value of the AC component of Vcrt.

6.4.3 Applicative solutions.

1) Fig. 31 shows the simplest solution in terms of components count. The current of the Line, wich is insulated form the Slic, is sensed through a dual optocoupler.

The ringing current is sensed by the LEDs and a push-pull structure to charge and discharge the capacitor is made up with the foto-transistors.

When the line current is positive LED1 switches on FT1 charging the capacitor CRT ; when negative, LED2 switches on FT2 , discharging CRT.

The calculation in 6.4.2) can be directly applied;only the VCEsat of FT1 and FT2 has to be taken in account as Vcc and Vss reduction.

2) Fig. 32 and Fig. 33 show a not insulated solution that, although requiring higher component count,features high rejection to the longitudinal current.

Figure 31.

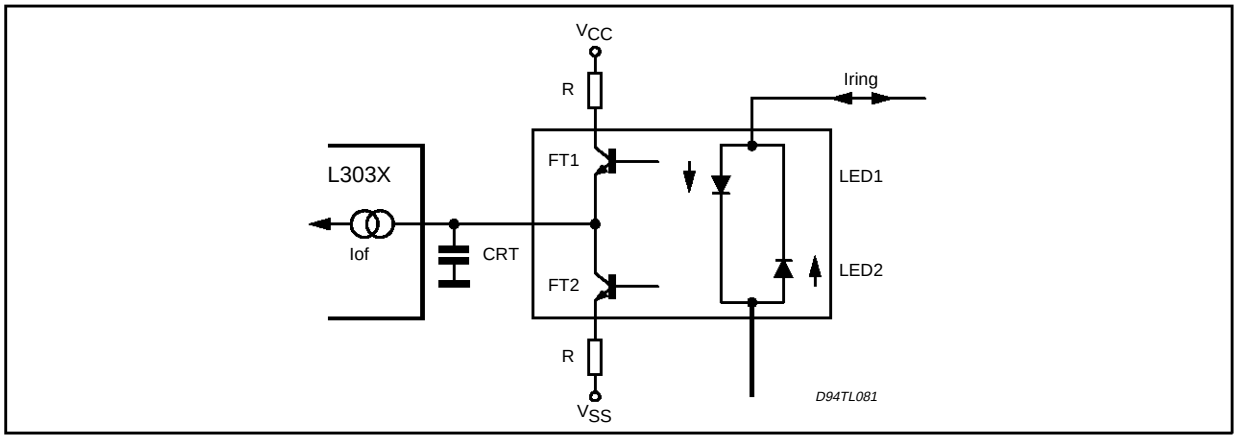


Figure 32.

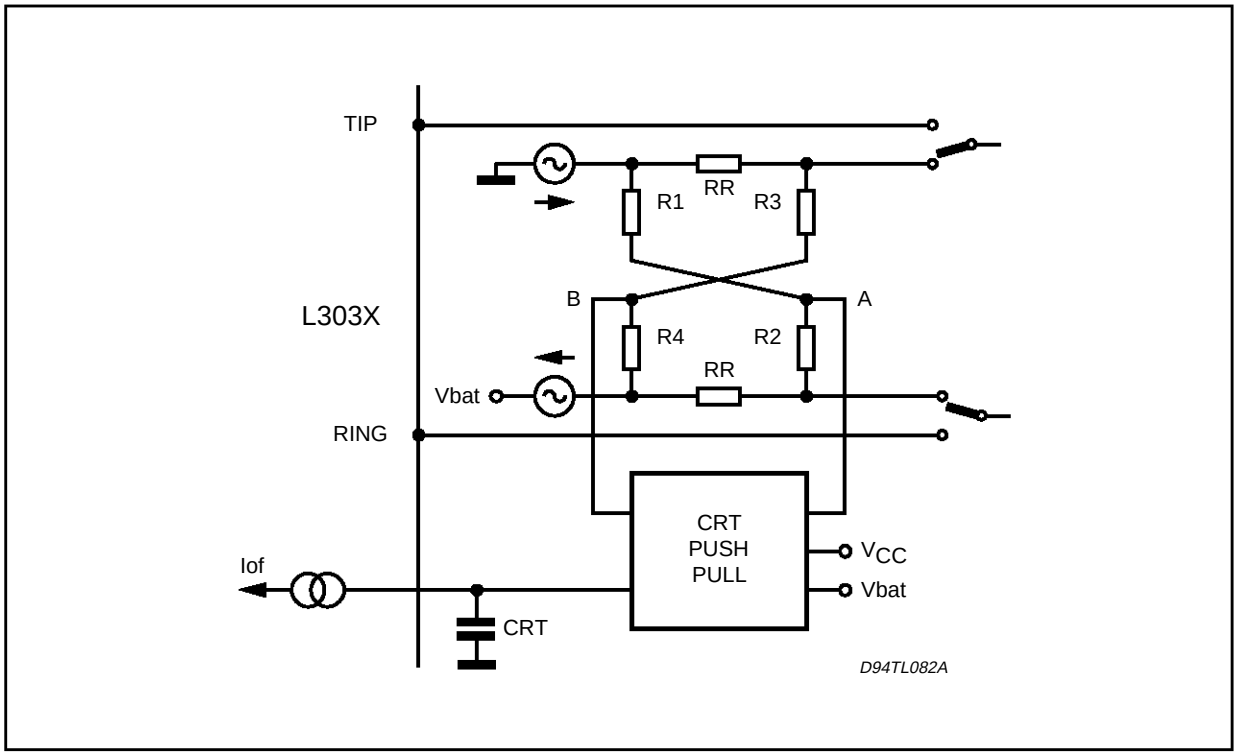
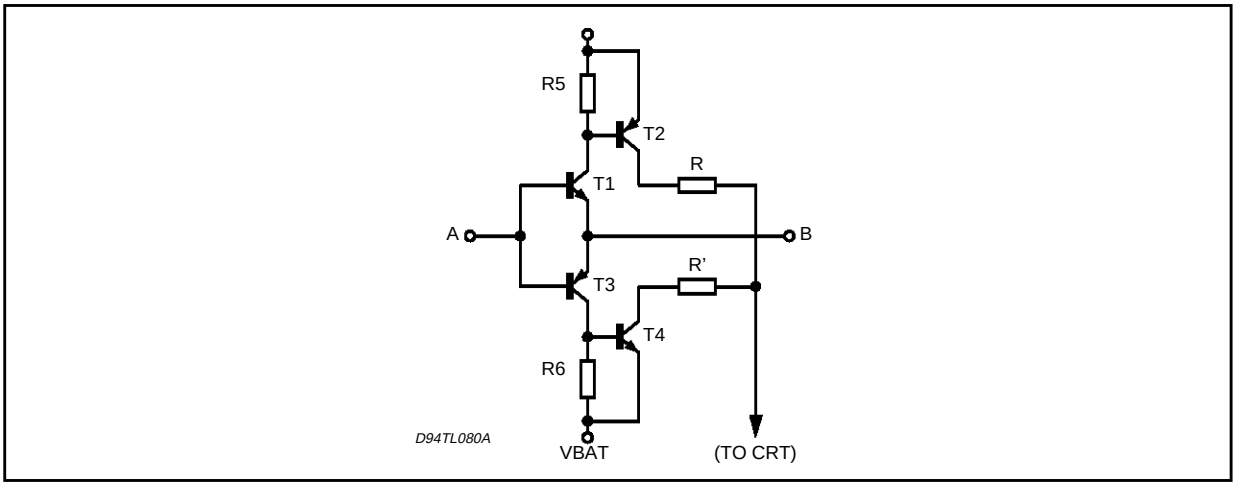


Figure 33: Balanced Ring Trip Detector 2. CRT Push Pull.



The bridge structure, R1/R2 and R3/R4,rejects the balanced AC voltage of the ringing generator at the nodes A and B,that are biased with a common mode DC voltage VA = VB = Vbat/2.
The differential voltage VAB= RR*Iring,is depending on transversal current only.
According to the direction of the Line current the transistors T1-T2 or T3-T4 charge or discharge the capacitor CRT.

In absence of ringing current the push-pull structure remains tri-state.

A and B nodes are biased at Vbat/2 and the negative supply of the push-pull is Vbat.

Procedure in 6.4.2) can be used again:

calculate CRT and R as though Vbat = -Vcc; then R' value is obtained by multiplying R by the factor Vbat / Vcc: $R' = R \cdot (Vbat / Vcc)$.

It's a first approximation value and in general a final adjustement is needed.

In order to minimize the power dissipation, R1 R2 R3 R4 must be high value resistors, compatibly with the capability to drive the push-pull.

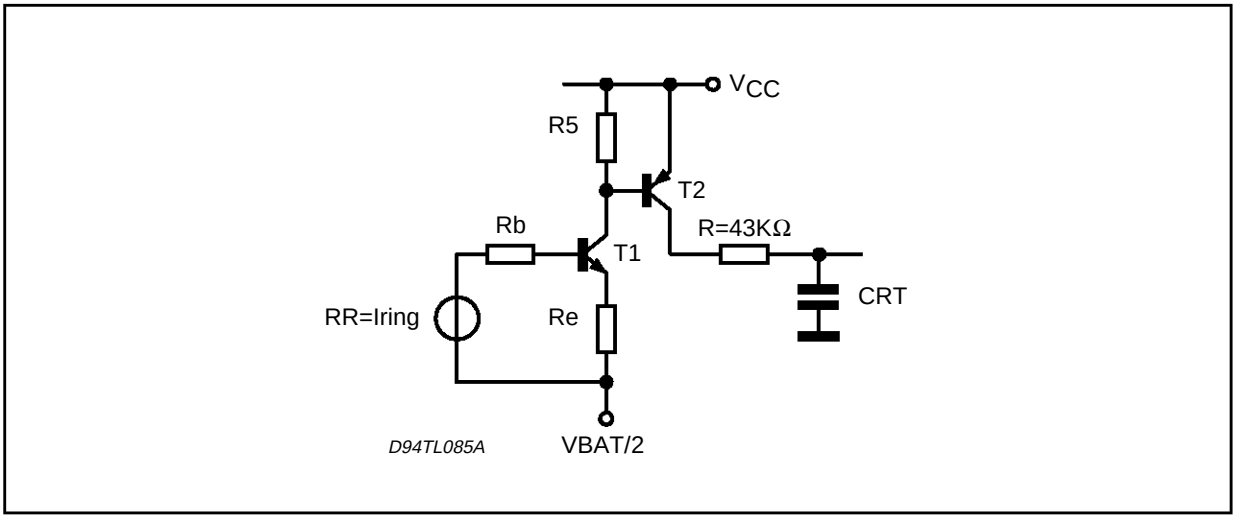
Example.

For calculation assume:

- hfe > 100 for T1 and T3 (linear operation)
  hfe = 10 for T2 and T4 (saturated operation)
- R5 = R6 = 300KΩ to maintain T2 and T4 in Off condition
- RR = 220Ω depending on the maximum ringing current allowed in case of short circuit.
- -Ith = 10mA minimum current sensed;below this threshold the push-pull remains tri-state.

Let's consider the CRT charging cycle; the equivalent circuit is shown in Fig. 34:

Figure 34.



were: Rb= R1 / / R2 and Re = R3 / / R4

Ic2 = (Vcc - Vce) / R = (5.0-0.2) / 43 = 112µA

Ib2 = Ic2 / hfe = 112 / 10 = 11µA

IR5 = Vbe / R5 = 0.7 / 300 = 2µA

Ic1= Ib2 + IR5 = 11 + 2 = 13µA

VABmin = RR · Ith = 220Ω · 10mA = 2.2V

disregarding the very low voltage drop on Rb:

VABmin = Vbe + (Re · Ic1)

and Re ≤ (VABmin-Vbe)/Ic1

Re ≤ (2.2 -0.7) / 13µA = 115KΩ

R2 = R3 = 2 · Re ≤ 230KΩ

Considering that in Rb flows a very low base current, R1 and R2 can be defined with higher value than R3 and R4.

The condition limiting the value is that the voltage drop Rb · Ib must be negligible respect to Re · Ie.

Rb = 2 · Re

can be used as a rule of thumb formula.

R1 = R2 = 2 · Rb = 4 · Re ≤ 460KΩ

With the calculated values the power dissipated by the bridge in stand-by condition is:

PWB = PW12 + PW34 = $Vbat^2$ / (R1 + R2) +
+ $Vbat^2$ / (R3+R4) = 2.5mW + 5.4mW = 7.9mW

Lower limit of the bridge resistance is defined by the maximum power dissipation PWB_{MAX} allowed.

R1 = R2 (3/2) · ($Vbat^2$ / PWB_{MAX})

R3 = R4 (3/4) · ($Vbat^2$ / PWB_{MAX})

7. POWER CONSUMPTION AND DISSIPATION.

In order to optimize the power consumption and consequentely the thermal dissipation, L303X Slic provides a regulation of the negative voltage VREG, with a series external transistor (see Fig. 35). This transistor, in addition to the VBAT ripple rejection, performs the basic function of sharing the power dissipation, reduces the amount due to the Slic and avoids, in most cases, the use of heat-sinks.

The power share depends on:

1)Rfeed (equivalent feeding resistance)

2)Line Resistance: that defines the operation point in the DC characteristic.

Fig. 36 and Fig. 37 show the power dissipation of Slic and ext. transistor as a function of the load (line resistance) for two DC feeding values:
Rfeed = 400Ω and Rfeed = 800Ω.

For a better understanding, some remarks have to be done. Referring to the DC characteristic:

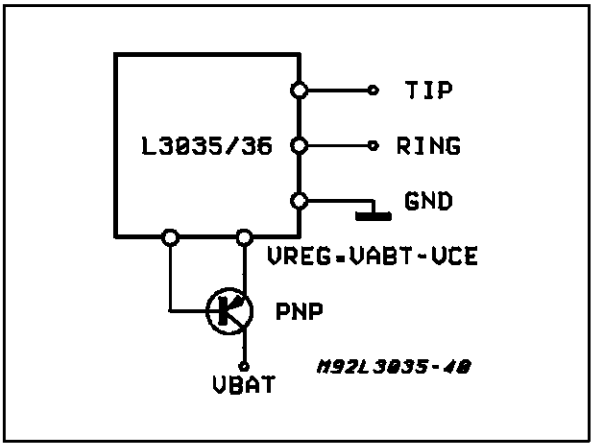
1)In resistive region (Il < Ilim) the transistor has a VCE = 1.7V indipendent from Il value. In that region the transistor dissipation is:

Ptr = VCE · Ic

It is very low (low VCE and low Ic)

Increasing the line current Ptr increases proportionally but much less than the Slic dissipation Psl.
In resistive region the thermal contribution of the transistor is not important.
The function of the transistor is only the rejection of the ripple on Vbat.

Figure 35.



2)Once the limiting region is reached Il=Ilim,the transistor acts as a current regulator.
As RL decreases VCE increases, with the result that Ptr increases and Psl decreases.

In other words this kind of regulation provides the Slic of a variable battery that adapts its voltage to the length of the line; the exceeding voltage drops on the external transistor.

As shown in Fig. 36 and Fig. 37 the Slic has the maximum dissipation at the limit of the two operating regions.
In this condition we have Il = Ilim and maximum voltage Vtp between TIP and RING.
With lower line resistance Il remains constant but Vtp decreases and, consequentely, the dissipation.
For the transistor the maximum dissipation corresponds to a short-circuit on the line. In such a condition we have Il = Ilim and maximum VCE on the transistor.

The worst case dissipation values depend on the value of the feeding resistance Rfeed.

At higher Rfeed values correspond higher Psl and lower Ptr values.
From the diagrams we can see for I_{LIM} = 43mA

1) Rfeed = 400Ω Psl = 700 mW Ptr = 1500mW

2) Rfeed = 800Ω Psl = 1400mW Ptr= 800mW

This point is important and has to be considered for proper definition of on-board heat-sink copper area and transistor choice (Rth).

Figure 36: Power Dissipation/1

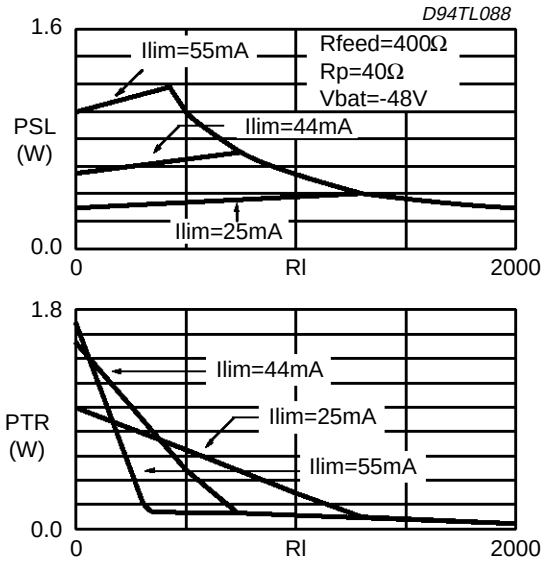
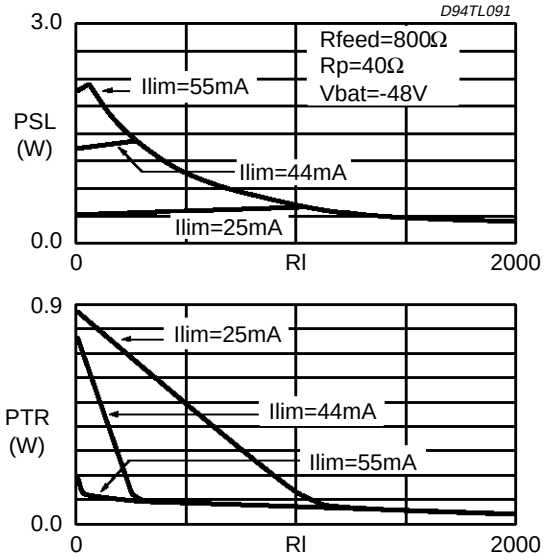


Figure 37: Power Dissipation/2



7.1 PACKAGE.

L303X is assembled in PLCC(34+10)
Ten pins, pin10 to pin14 and pin32 to pin36, are an extension of the frame and give a good contribution to heat dissipation when soldered to an on-board heat-sink.

Fig. 38 and Fig.39 show the diagrams:

Figure 38: PLCC 34+5+5 - Rth(j-a) on PCB vs PCB heat sink.

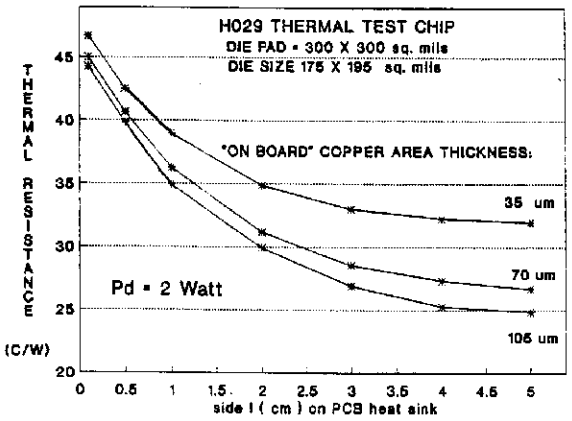
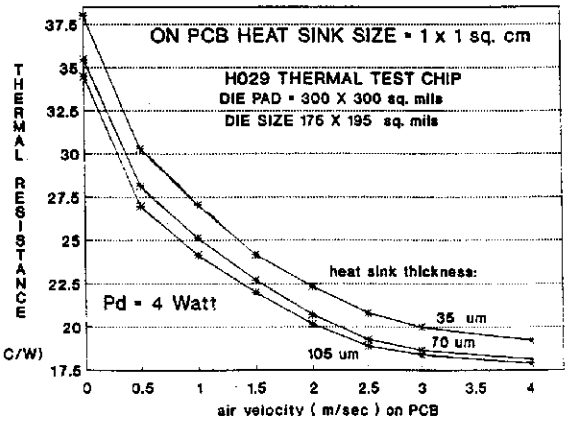


Figure 39: PLCC 34+5+5 - Rth (j-a) vs. air flow.



EXAMPLES:

ex1: Ilim = 25mA, Rfeed = 800Ω, Tamb = 50°C
Pd = 580mW
Supposing no heat sink on PCB and no air flow:
Rthj-a = 45°C/W ---> Tj = 50+45 · 0.58 =
= 50+26 = **76**°C

ex2: Ilim = 43mA, Rfeed = 800Ω, Tamb = 50°C
Pd = 1480mW
Supposing l = 1cm heat sink on PCB and no air flow:
Tthj-a = 36°C/W ---> Tj = 50+36 · 0.58 = **103**°C
Supposing l = 1cm heat sink on PCB and 0.5m/s air flow:
Rthj-a = 27.5°C/W ---> Tj = 50+27.5 · 1.48 = **90.7**°C

ex3: Ilim = 56mA, Rfeed = 400Ω, Tamb = 50°C
Pd = 1200mW
Supposing l = 1cm heat sink on PCB and no air flow:
Tthj-a = 36°C/W ---> Tj = 50+36 · 1.20 = **93**°C
Supposing l = 1cm heat sink on PCB and 0.5m/s air flow:
Rthj-a = 27.5°C/W ---> Tj = 50+27.5 · 1.20 = **83**°C

8. OVERVOLTAGE PROTECTIONS.

8.1 LIGHTNING PROTECTIONS.

The protection against lightning is obtained suppressing to GND the surges, positive and negative, by a transient voltage suppressor TVS, directly connected to TIP and RING pins of L303X (see Fig. 40).

Positive surges are suppressed to GND by a clamping Diode and negative are suppressed to GND by a Thyristor.

The protection IC suggested, is a single chip dual suppressor, programmable type: Thyristor starts coducting when the voltage on the wire (TIP or RING) goes below the potential of the GATE.
In the application the GATE in connected to VBAT.
The thyristor is switched-on when the current reach the firing threshold.

The structure and electric characteristics is according to Fig. 41 and 42.

To meet different assembly needs it's available in three different plastic packages:

IC	PACKAGE
LCP150S LCP1511 LCP1512	SIP-4 SO-8 MINIDIP

Refer to LCP15XX Data-Sheets for more detailed information.

Figure 40.

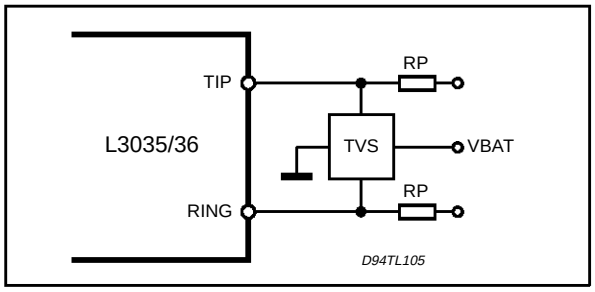


Figure 41.

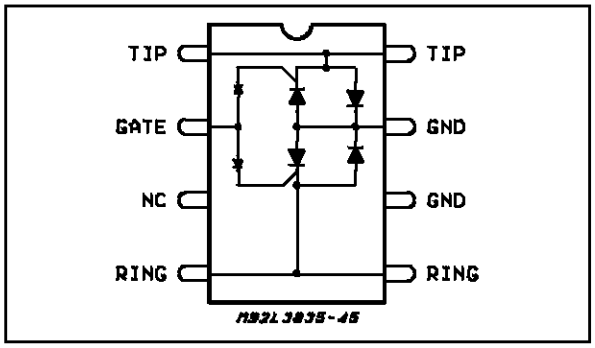
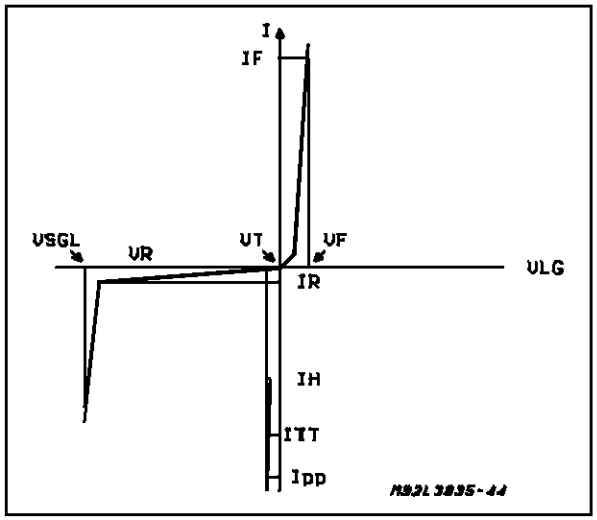


Figure 42.



8.1.1 Note.

During positive or negative surges the current flowing through the suppressor is mainly limited by the two RP resistors that dissipate most of the surge energy .

Suggested RP type are 2W wire wound resistors or thick film resistors on ceramic substrate.

8.2 POWER-CROSS PROTECTION.

In case of power-cross a long time overvoltage, continous or intermittent, is applied to the line.

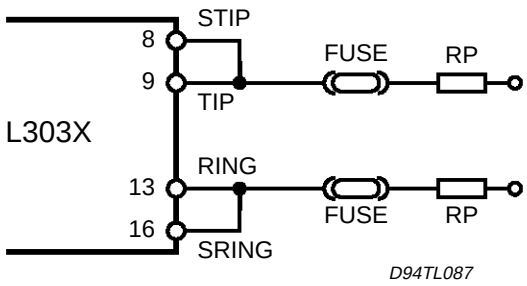
Specific protection has to be provided: lightning protection can absorbe fast transients only and a long duration event like a power-cross will burn it out.

Typically two different solutions can be adopted:

1) Fuse:
in series to each wire is provided a fuse that opens when the current exceeds a certain value.
Besides a proper fusing current, a sufficientaly long thermal time-constant is required, in order to withstand lightings; on the contrary, maintenance intervention will statistically increase.
Typically it's a metal strip that take place on the same ceramic substrate of the protetction resistors.

In this case the feedback for PTCs mismatch compensation is not necessary.
STIP (Pin 8) can be directly connected to TIP (Pin 9) and SRING (Pin 16) to RING (Pin 15) see Fig. 43.

Figure 42.



2) PTC:
another solution widely adopted is to put PTCs in series to the line wires.
In case of high current injection when the PTC, after a thermal transient, reaches a sufficiently high temperature (tripped state) its resistance highly increases limiting the injected current, preventing the damage of the Slic and lightning protection.

The value of the resistance in trip condition depends on the overvoltage level.
Under power-cross condition the injected power is mainly dissipated by the PTCs.

PTCs have not to trip in the operating current range of the Slic and in tripped state the dissipation of the Slic and TVS has to stay below the maximum allowed.

An aspect to be considered is the transient time.
During the transient, before the trip condition, the power is mainly dissipated inside the Slic and TVS.
The temperature of Slic and TVS increases till the tripped state is reached and its maximum value is related to the ratio of the time-constants.
If the transient takes too long, Slic and TVS can be damaged before the tripped state is reached.
As a general rule the PTC has to be the fastest.

To evaluate power dissipation in the Slic and protection, before the PTCs trip consider that:

1) Slic: TIP and RING can sink or source a maximum current of 100mA; exceeding current flows through the protection IC.

2) Protection IC: when the positive half-wave goes over GND the overcurrent flows through the clamping diode and the power dissipation is $PD = I \cdot Vf$.
When the negative half-wave goes below VBAT the current flows through SCR not yet fired the dissipation is at the maximum level : $PD = I \cdot Vsgl$.
When the current reaches the firing threshold the power dissipation becomes: $PD = I \cdot Vt$.

8.3 CONCLUSIONS

Fig. 43 and 44 shows the typical configuration for L303X SLIC protection with fuse or PTC, solution used in fig.43 can be used also replacing fuse with PTC, but in this case the PTC mismatch is not compensated, therefore the longitudinal balance performance of the application will depends on the PTC matching value.
Refer to device datasheet for the components value.

Figure 43: Typical Application Circuit with Fuse

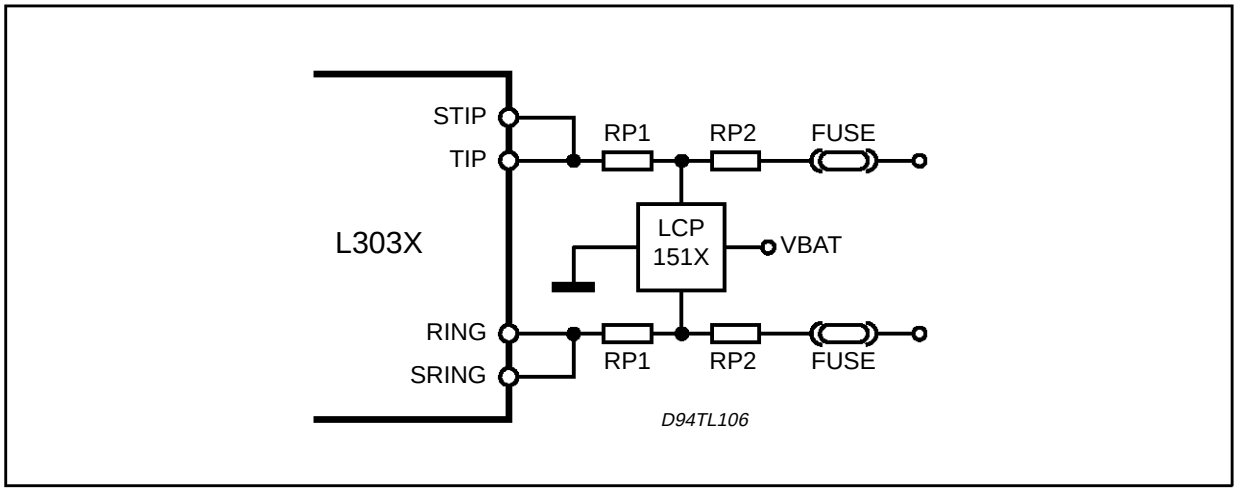


Figure 44: Typical Application Circuit with PTC